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QST Issue: Oct 1981
Title: CMOS Super Keyer, The
Author: Jeffrey Russell, KC0Q

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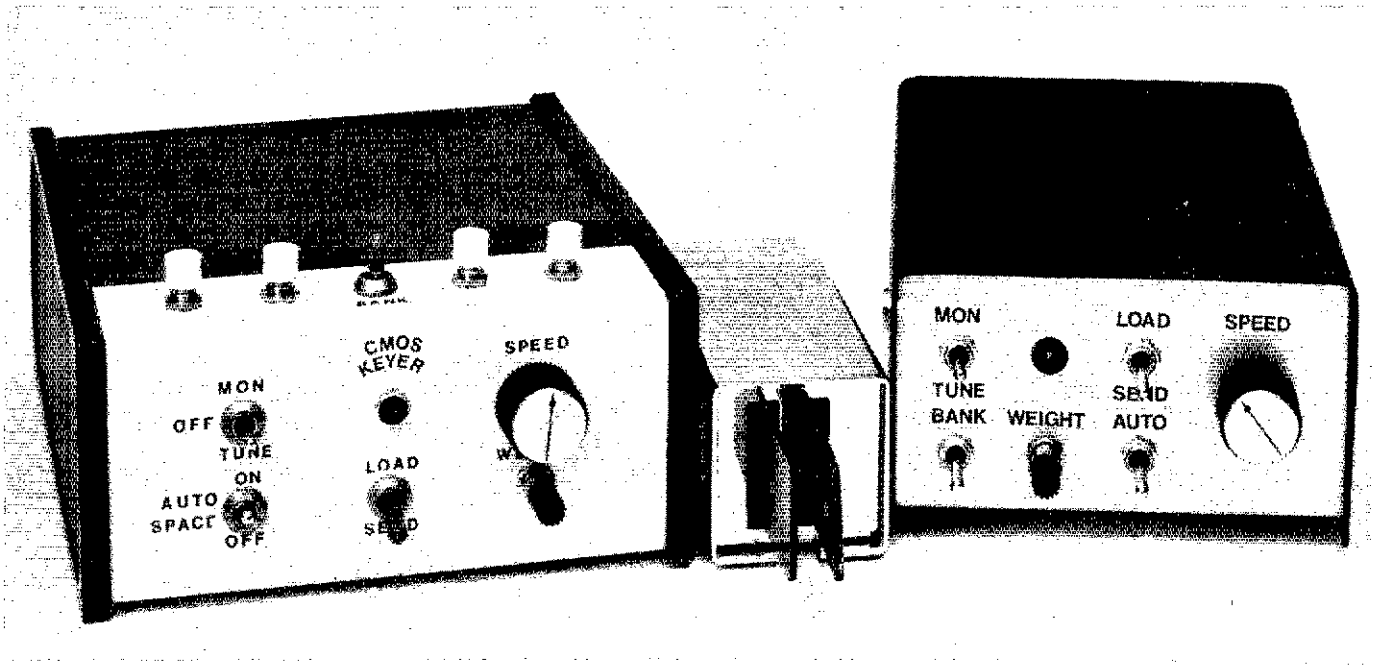
The CMOS Super Keyer



Able to bridge tight pocket books with a single board, this keyer has a features/cost ratio that is hard to beat! It is designed for — and by — cw operators.

By Jeffrey D. Russell,* KCØQ, and Conway A. Southard,** NØII

Why should *you* build this keyer? Well, let's start by listing its prominent features, and see if you can resist its attraction: (1) Compact and inexpensive; (2) Has eight 50-character message memories; (3) Messages are loaded or aborted by paddle operation; (4) Transmitter not keyed during message loading; (5) Any message may be instantly restarted; (6) Includes a message loading indicator; (7) Incorporates iambic operation; (8) Employs both dot and dash memories; (9) Has switch-selectable, auto-character spacing; (10) Uses a gated clock for instantaneous asynchronous starting; (11) Has ultra-low power requirements; (12) Features continuous message retention; (13) Offers very friendly timing circuitry.

Not only will you have a keyer that you will be proud of, but those interested in logic design will find this presentation useful and interesting. Several novel features help to reduce the number of ICs used — only 12 readily available ICs are required. CMOS devices are employed, and with no quiescent current paths the keyer draws only 10 to 15 microamperes in standby. It has no ON/OFF switch! A state transition diagram is also included and, as far as we know, it is the first keyer so presented.

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Cost

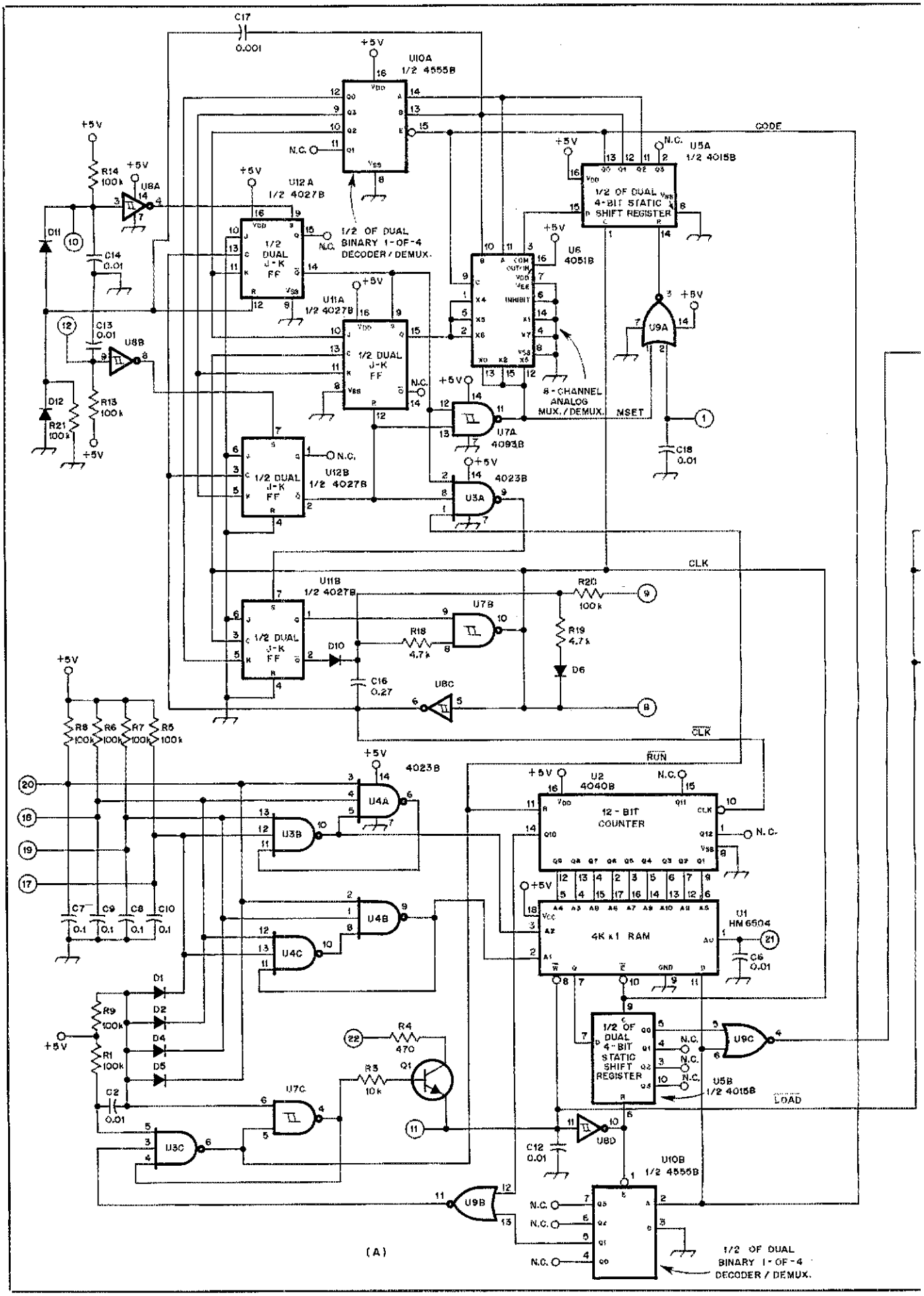
Certainly this is a factor of primary concern to amateurs. Total IC costs will be about $10, including an approximate cost of $7 for the RAM chip. If your junk box is helpful, a total cost of $20 or $25 can be expected. If you need to buy all the parts,[1] the keyer could cost $60 or so. Not bad in light of today's "smaller" dollar. Double-sided pc boards with plated-through holes are available from either author at a cost of $15 each (plus $1 shipping).[2] These boards measure 3.6 × 4.6 inches (91 × 117 mm).

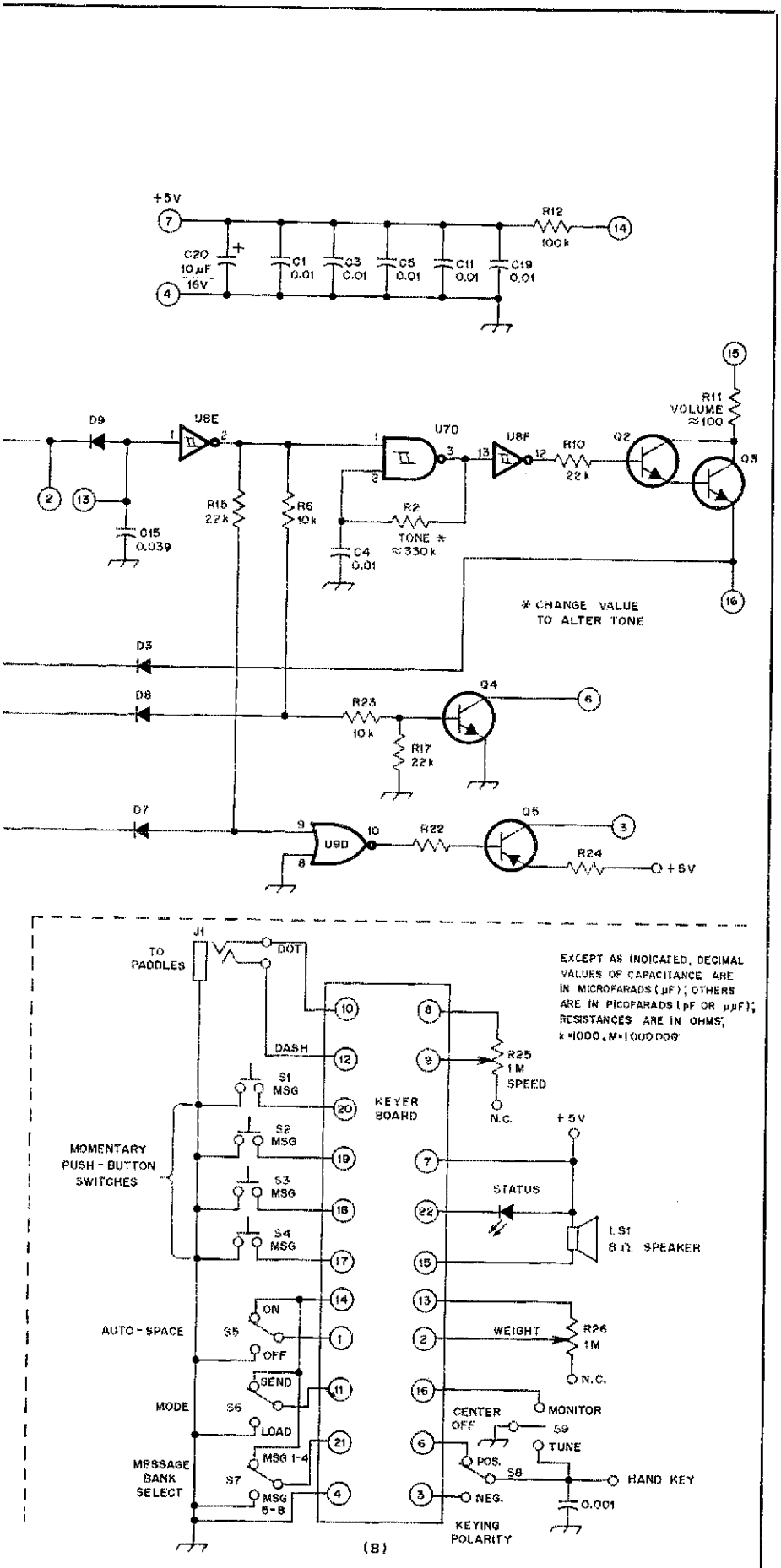
[1]Notes appear on page 17.

CMOS Design

The advantages of CMOS technology are apparent in this keyer: low cost, ultra-low power requirements, wide logic swings, "down-the-middle" transfer characteristics, high impedance inputs, lots of "fan out" drive capability and good noise immunity, to name a few. The 6504 RAM can store 4096 bits: that's eight messages of 512 bits each, or about 50 characters per message.

This circuit does not depend on how fast one IC is with respect to another. In some designs you are instructed to swap this or that IC if you have a problem, or R-C networks are added to the circuit to reduce "glitches" or race conditions. There are no R-C de-glitchers in this design. The read-in/read-out memory-





address transitions are logically synchronized, and all transition states are provided for.

Functional Keyer Description

There are four basic areas of the keyer: The ASYNCHRONOUS paddle logic and oscillator, SYNCHRONOUS (state machine) section, MEMORY AND MEMORY CONTROL, and the WEIGHTING, OUTPUT and SIDETONE section (discussed under Wiring Options). We'll examine them one at a time.

Asynchronous Module

Almost all modern keyer designs have dot and dash memories, as does this one. However, many designs don't allow the full time between elements to get off the dash or dot paddle before another element is loaded. The result, for those keyers, is that you may have difficulty with extraneous elements (usually dots) creating, for example, an R for an A or an I for an E. This keyer design allows you the full interelement time to release the paddles, and a special dot reload circuit makes squeeze timing even less critical — it is a super-easy keyer to use.

The ASYNCHRONOUS module derives its name from the fact that paddle manipulation by the operator can be, and usually is, quite irregular and not in phase with any internal keyer clock. Refer to Fig. 1. U8A and U8B are inverters that isolate the dot and dash paddles. U12A and U12B comprise the dot and dash memory FFs (flip-flops). These FFs are set by the action of the paddles and are reset (as described later) by the state module or the SYNCHRONOUS section. U11A is the iambic FF that allows the keyer to provide alternate dots and dashes when both paddles are closed. (Iambic operation seems to be the design preferred by most

Fig. 1 — Schematic diagram of the keyer. One-eighth- or 1/4-watt carbon resistors should be used. Simplification of the keyer by elimination of features and by component selection is discussed in the text. The circled leads at A correspond to the board edge connector pads shown at B. With the exception of C15, C16 and C20, all capacitors are disc ceramic, 50-V units.

C15 — Mylar, 0.039 µF, 50 V.
C16 — Mylar, 0.27 µF, 50 V.
C20 — Electrolytic or tantalum, 10 µF, 16 V.
D1-D12, incl. — Silicon, fast-switching diode, 100 PIV, 75 mA, 4 ns, 1N4454, 1N914, 1N4148 or equiv.
Q1-Q3, incl. — Npn silicon low power, general-purpose amplifier, 500 mW, 2N2222 or equiv.
Q4, Q5 — See text.
U1 — CMOS 4k × 1 RAM, Harris HM6504-9.
U2 — CMOS 12-bit counter, 4040B.
U3, U4 — CMOS triple 3-input NAND gate, 4023B.
U5 — CMOS dual shift register, 4015B.
U6 — CMOS 8-to-1 multiplexer, 4051B.
U7 — CMOS quad Schmitt NAND gate, 4093B.
U8 — CMOS hex Schmitt inverter, 40106B, MC14584B.
U9 — CMOS quad 2-input NOR gate, 4001B.
U10 — CMOS dual 2-to-4 decoder, 4555B.
U11, U12 — CMOS dual J-K FF, 4027B.

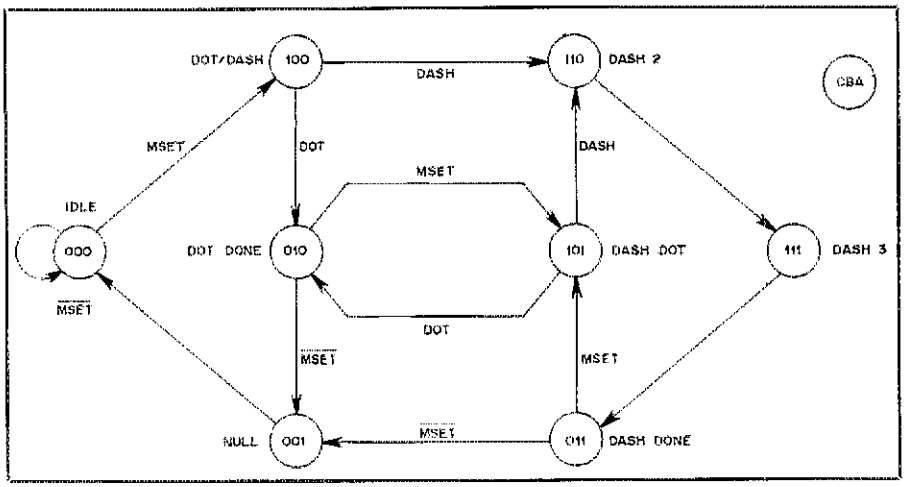


Fig. 2 — State transition diagram of the keyer. Dot = not dash, dash = current output of the iambic FF, MSET = 1 if either the dot or dash memory is set. At the completion of a dot, state 010 (dot done) is always entered. After dash completion, state 011 (dash done) is always entered. A mark is begun in either state 100 or 101. The clock produces short negative-going pulses, and all state transitions occur on the positive-going clock edge. An attempt is made to reset the dot memory on the negative clock pulse edge during the end of state 010 and to reset the dash memory on the negative clock edge during the end of state 011. Setting of the iambic FF to dash on the transition from state 010 to 101 and resetting to dot on transition from 011 to 101 is sought. If the dot reload timing change described in the text is used, a special dot reset pulse is generated at state 110, which tries to reset the dot FF.

Table 1

Edge Connector Signals

Pad Number	*Signal*
1	AUTO-SPACE
2	WEIGHT (1)
3	Negative keying output
4	Ground
5	Spare
6	Positive keying output
7	+5 V
8	SPEED (1)
9	SPEED (2)
10	Dot paddle input
11	LOAD switch
12	Dash paddle input
13	WEIGHT (2)
14	Positive high for pull-ups
15	Speaker
16	MONITOR switch
17	Message button 4
18	Message button 3
19	Message button 2
20	Message button 1
21	MESSAGE BANK SELECT switch
22	STATUS LED

operators.) FF U11B is set to turn on the gated oscillator and keeps the oscillator running until it is stopped intentionally.

The oscillator, U7B and U8C, is gated so that a character can start immediately when you close a paddle. Some designs with gated clocks have a first cycle that is not the same length as the succeeding ones. This problem may be solved by using a continuously running clock, but creates another problem: A character may be initiated only at some undetermined time after paddle closure, depending on where the oscillator may be in the cycle at the time. The oscillator in this keyer is gated, and, when stopped, its output (CLK) is high. Further, the duty cycle is purposely set with a very short negative pulse and a long positive pulse that eliminates the "first-cycle" syndrome. This is crucial to the overall operation of the keyer. D10 serves as a precharge path for the oscillator; it ensures that the oscillator returns quickly to the idle state at the end of the keying cycle.

The dot and dash FFs are set by the paddles, and their outputs are combined in gate U7A. U7A output is the signal called MSET (Memory SET) on the state transition diagram and is a 1 if either or both FFs are set. The MSET signal is an input to the state module. The output of iambic FF U11A is called DOT/DASH and will be a 1 for a dash or a 0 for a dot. The J-K FF used at 11A must have a defined state when both SET and RESET are active — not all FFs are acceptable here.

Dot and dash FFs U12A and U12B are reset by the CLK-NOT (the negative going edge of CLK) on leaving state 010 for a dot or 011 for a dash. These same signals are used to toggle the iambic FF, too.

Clock FF U11B is turned on by a dot paddle closure, a dash paddle closure or a RUN-NOT signal from the memory section. This FF is reset by a high on the K input, which occurs only at state 000, when the keyer has arrived at the idle condition. The oscillator (U7B/U8C) normally does not have a linear speed characteristic, but this is relieved by using a SPEED potentiometer with an inverse log taper. A regular log (audio) taper potentiometer may be used here, but should be wired to increase speed with a counterclockwise rotation of the control.

Synchronous Module

This is the heart of the keyer logic. A state transition diagram (shown in Fig. 2) will aid in explaining the sequencing of the keyer. Basically, the circuit operates as a clocked-state machine with eight states. These states are identified in binary code (CBA), and the circle nodes on the diagram are the binary description of the states. States are identified out of a shift register, which is always shifting to the right. For example, the state 000 is the idle state and when either paddle is closed, the state shifts right and a 1 is shifted into the first position (C) — hence the state 100. Keep in mind that whenever the C position is a 1, the keyer will be outputting a MARK. So on closure of either paddle, the keyer sequences to state 100, and a MARK is output.

On the next clock tick, the keyer can move to state 010 or 110, depending on which desired element (dot or dash) is being keyed. Note that the state is shifted right, and a dash will cause a 1 to shift into the register for state 110, or a not-dash (dot) will cause a 0 to produce a state 010.

In general, a state machine must have sufficient memory to determine its past history (to know what state it is in) that, when mixed with input signals (called qualifiers), will exactly determine the next state. The state history for this unit is kept in a 4-bit shift register, U5A. U5A is clocked (shifted right) by CLK, and the left-most bit is loaded into the D input from U6. The state of the keyer is determined by Q0, Q1 and Q2, and these outputs are the CBA node identifiers in the state diagram. The fourth bit of that shift register is ignored, as only three bits are needed to define the eight states of the keyer.

Assume the keyer is in state 000, and a clock pulse occurs. The signal at U6 input X0 (pin 13) will be output at pin 3 and will become the first bit shifted into the register. Since the clock pulse must occur because of a paddle closure, MSET at pin 13 will be a 1, and the shift register is now set at 100.

Because of this action, the keyer will go to state 100 from 000 with any paddle closure. However, the next state will either be 010 or 110 depending on the DASH input (refer to the state diagram in Fig. 1). Which inputs to U6 are coupled to the shift register are determined by the current state of the keyer and these inputs.

A single dot closure of the paddle produces the following states: 000 (idle), 100 (send dot/MARK), 010 (dot done), 001 (null) and back to 000 (idle). A dot in state 100 is sent, and then the keyer inserts three space elements — the AUTO-SPACE feature.

To produce a single dash, the states are: 000 (idle), 100 (send dash/MARK), 110

(send second MARK), 111 (send a third MARK), 011 (dash done), 001 (null) and 000 (idle) again. A dash is three elements long, followed by three spaces for AUTO-SPACING.

The dot-done (010) and dash-done (011) states test for the MSET line and controls the sequence and alternating requirements for iambic operation. MSET indicates that *either* the dot or dash memories have been loaded. The signals DOT and DASH just indicate whether the dot or dash memories have been set.

The state outputs of U5A are fed to U10A, an output decoder. U10A produces an output at pin 12 for state 000, which is used to attempt a reset of FF U11B and to turn off the clock. For state 010, an output at pin 10 attempts to reset the dot FF and/or toggle the iambic FF U11A. An output at pin 9 for state 011 attempts to reset the dash FF and/or toggle the iambic FF.

U9A supplies a reset signal to the shift register U5A. With the AUTO-SPACE on, a reset is never applied. With AUTO-SPACE off, a low on MSET will cause U5A to reset and return immediately to the idle state. This can only occur at dot-done (010) or dash-done (011) if no paddle is closed; the state module will be short circuited to idle through those two states. All other valid states will have an MSET signal except dot-done or dash-done. AUTO-SPACE OFF prevents the keyer from cycling through the three nulls.

Message Memory and Control

The inclusion of message memory is almost a requirement for cw operation. Therefore, message memory was designed as an integral element of the total design. This circuit includes the RAM (U1), a sequence counter (U2) and some control circuitry — a "which button has been pushed" latch and decoder (U4A, U3B, U4B and U4C), a cross-coupled FF and message-initiate circuit (U7C, U3C), U5B, U10B, and a couple of gates.

U4A/U3B and U4B/U4C are cross-coupled R-S FFs. Pushing a memory button will set these FFs into one of four states, and the outputs are directed to two address lines of the RAM. One address line from the RAM goes to the BANK SELECT switch, which accounts for three of the 12 address lines. The other nine lines come from the counter, which can then count up to 512 bits (about 50 characters) per message.

The tenth line out of the counter is used as an end-of-buffer signal, which resets FF U7C/U3C; this FF is a message-in-progress FF. Decoder U10B is wired so that if the LOAD/SEND switch is in the SEND position and a code element from the keyer arrives on the CODE line, U10B Q1 output will stop the memory. U9B ORs the stop conditions so that the messages terminate by counting up to 512 or when a paddle has been closed. FF U7C/U3C is set through the diode bank (D1, D2, D4, D5) if any button is pushed.

C2 has a special function. If the memory is already running, RUN-NOT will be low, and a pushed button actually forces FF U7C/U3C to a temporary one-shot condition. This provides a pulsed high on the RUN-NOT line and resets the counter to zero. Without this capacitor, restarting a message from the beginning would be impossible.

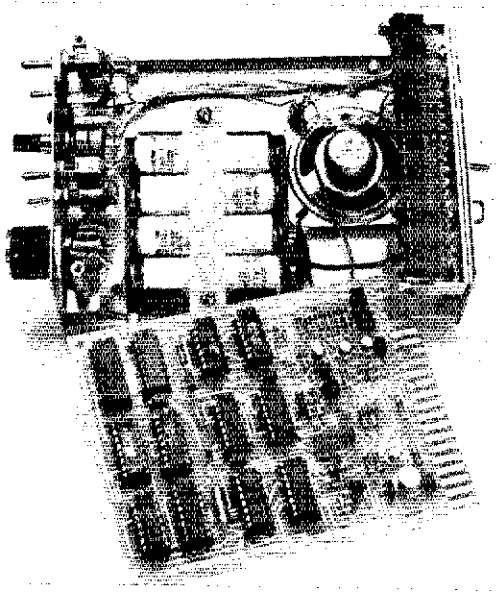
U5B has a unique function, too. It's clocked by the CLK line, which is the same signal that is used to enable the RAM. The rising edge of CLK loads U5B with the data read from memory and holds it for the whole cycle. This way, the RAM can return to standby, and any glitches that might occur in the output, as the address lines are changing, are effectively masked. The counter is incremented by the CLK-NOT signal and is therefore positioned and ready for the next read cycle.

Construction

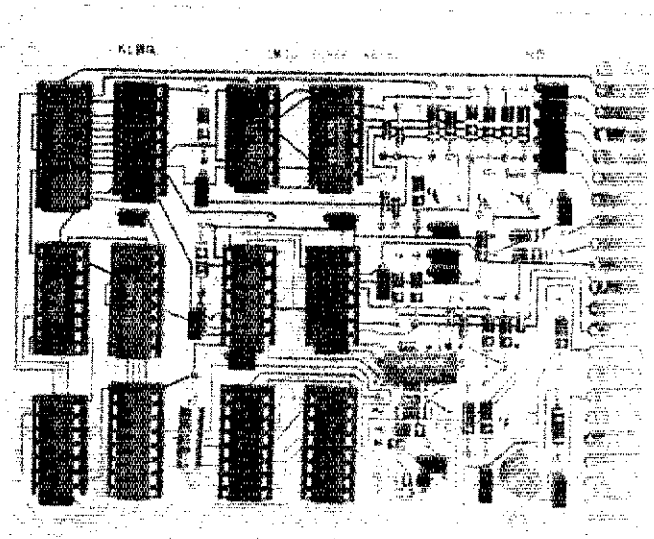
Point-to-point or wire-wrap methods can be used to construct the keyer, but a printed-circuit board is available. With the board, use sockets for the ICs and solder the components to the board while using a low-wattage soldering iron, employing a minimum of heat and solder. The board is laid out with the ICs all oriented in the same direction and with component numbers assigned for easy identification. There are leads between IC pins on the component side of the board, to reduce the physical size of the board. Be careful not to create solder bridges.

This board is designed for use with a standard 22-pin edge connector or solder pads for interconnection to off-board components. Two mounting holes are provided opposite the edge connector. If the edge connector is not used, a third mounting hole can be drilled between pads 4 (ground) and 5 (spare).

It is recommended that you remove the solder flux from the pc board after mounting the components. Radio Shack rosin flux remover (64-2324) is readily available for this purpose. CMOS has



An inside view of the KCØQ keyer. A 10-position switch and associated fixed-value resistors are used for the SPEED control. The 22-pin edge connector is secured to the rear panel by means of a homemade hinged bracket, allowing easy removal of the pc board.



A closeup of the component side of the double-sided pc board. All ICs are oriented in the same direction — a nice touch! If the use of an edge connector is not desired, interconnections may be made by use of holes already drilled at the inside edges of the edge connector pads.

high-impedance inputs. While new, dry solder flux is a good insulator, moisture and other contaminants may create problems later.

Wiring Options

Speed Control: Keyer speed increases as the resistance of R25 decreases. For best operational linearity, the SPEED potentiometer should be an inverse-log taper unit. If counterclockwise rotation of the control is acceptable when increasing speed, a log taper potentiometer will suffice. An alternative to using a potentiometer is the use of a multiposition rotary switch and selected fixed resistance values. Eight or 10 rates of speed are often adequate for normal operation. The resistor values must be chosen experimentally, because the speed is determined by the value of resistance used for R20, R25 and the value of C16; C16 may have a value different from the one marked.

Weight Control: Control of weighting is accomplished by means of D9, C15 and R26. A log taper potentiometer is recommended in order to obtain a finer degree of control at the low-resistance end of the range (as might be used at high keying speeds). The maximum amount of weighting obtainable is determined by C15; the value may be changed to suit your preference. If a weighting control is not desired, eliminate R26, C15 and D9, and install a jumper in place of D9.

Auto-Space Select: S5 may be eliminated if switch selection of the AUTO-SPACE feature is not desired. To disable AUTO-SPACE, don't use C18; install a jumper instead. To enable AUTO-SPACE continuously, disregard C18 and install a jumper between edge connector pads 1 and 14.

Message Bank Select: To limit the number of messages to a bank of four, leave out S7 and C6. Install a jumper in place of C6.

Monitor On While Loading: D3 provides a path to turn on the internal monitor automatically while loading messages. If this is not desired, eliminate D3.

Output Inhibit During Loading: D7 and D8 serve to inhibit keying output when the MODE switch (S6) is in the LOAD position. These diodes may be omitted to delete that function.

Monitor Tone and Volume: The monitor audio frequency can be adjusted by changing the value of R2. Decrease the value of R2 to increase the frequency. If you do not need the monitor, you may exclude LS1, R2, R10, R11, C4, Q2 and Q3, and install a jumper in place of C4.

Dot Reload Timing Change: The dot-memory timing can be altered if desired. D11, D12, C17 and R21 delay setting of the dot FF for one baud during the sending of a dash. In the iambic mode, this allows the operator a bit more time to release the dot lever before the dot memory FF is reloaded. If you wish to delete that function, remove the aforementioned components and install a jumper in place of R21 or D12.

Output Keying: Most applications do not require positive and negative keying outputs. Either one may be disabled. For negative keying output only, eliminate S8, D8, R16, R17, R23 and Q4. If positive keying only is desired, omit S8, D7, R15, R22, R24 and Q5, and install a jumper in place of R15.

In the positive keying line, R16, R23 and R17 have been chosen to accommodate a wide range of keying circuits. Q4 must be selected to handle the keying circuit voltage and current requirements demanded by the transmitter.

Negative Keying Considerations

If negative keying lines are encountered, use the following procedure. Measure the key-up voltage and key-down current of the transmitter keying line. Select a transistor (Q5) that will handle the voltage present (with some margin of safety) and determine the beta of the transistor. Then calculate the values of R22 and R24 using the following formulas:

$$R22 = \frac{0.3 \times \text{beta (Q5)}}{I} \qquad \text{(Eq. 1)}$$

$$R24 = \frac{3.5}{I} \qquad \text{(Eq. 2)}$$

where

I = key-down current in amperes.

With some values of R22 and R24, the negative keying line can actually be pulled above ground potential by a small amount. Most transmitters can handle this positive voltage with ease. If you wish, a protection diode may be added between board pad 3 and ground. This will limit the voltage to one diode drop. Orient the diode with the anode at pad 3 and the cathode to ground.

Troubleshooting

Barring construction problems, bad components or early component failure, few problems (if any) should develop during the life of the unit. An oscilloscope is a useful fault-finding aid, but an analog voltmeter will suffice in many instances. With the analog meter, use the lowest SPEED setting and turn the WEIGHT control off. Higher SPEED control settings are more desirable when using an oscilloscope.

Pay careful attention to which section of the keyer is inoperative. For example, if an output code is present at pin 2 of the edge connector, don't examine the state machine while troubleshooting a monitor problem. If you have troubles in the memory section, check to see that clock pulses are appearing at U1 pin 10, U5B pin 9, and so on. The RAM WRITE line (pin 8) should be high or low depending on the setting of the LOAD/SEND switch. FF U3C/U7C should be set (U3C pin 6 low) when any message button is pushed, and the memory address lines at U1 pins 2 and 3 should indicate which button has been pushed. Otherwise, examine U4A, U3B, U4B and U4C for difficulties.

Remember, most problems are caused by improper construction or faulty components. If sockets have been used for the ICs, substituting and/or swapping ICs may help in locating the difficulty. Constructing the unit so that you can get to both sides of the board readily will make debugging much easier.

Operational Considerations

When power is first applied to the keyer, a continuous mark may be sent. This occurs because the current memory state contains a mark. Place the MODE switch in the LOAD position and depress one of the message buttons to clear the condition. It is recommended that *all* message buffers be cleared initially by setting the SPEED control to maximum and loading spaces into each buffer position.

Message Organization

The 6504 CMOS memory IC has 4096 bit positions that can be used to store data. Because each character requires approximately 10 bits, there is room for about 400 characters. This memory is organized as eight messages of approximately 50 characters each. Instead of using eight message switches, there are four push-button switches and one MESSAGE BANK SELECT switch, S7. (One husband and wife team actually uses the BANK switch to separate his/her messages!)

Loading Messages

Position S7 to select the desired message bank. Place the MODE switch in the LOAD position and start entering data from the paddles after pressing the appropriate message button. The STATUS LED will stay on until the memory is full. It is essential that you allow the keyer to continue loading until the LED extinguishes, even if you are not inputting data. On occasion, you may have a message that is too long for the buffer, in which case you will lose part of the message. It is also possible to leave a mark in the very last buffer location, which will condition the keyer to send a continuous mark if that message is played to the end. The latter condition is rarely encountered, but indicates a message that is a trifle long; it should be re-entered. Note: During loading, the internal clock is running continuously, and the message entered will have long character/word spacing if that is the way it was entered.

Message Playback

To output a loaded message, ensure the

MODE switch is in the SEND position and press the appropriate message push-button. Message output will continue until one of the following conditions occurs: the message buffer empties, a paddle closure occurs, or the same or another message push-button is pressed. Any message may be replayed instantly.

Power-Supply Considerations

Battery operation is recommended for this keyer because it provides continuous memory retention. You'll never need to reload the memories until a change is desired, a feature highly valued by most cw operators. While some operators have used four series-connected alkaline or zinc-carbon batteries, a better choice is a similar combination of NiCads. Using 450 mAh (milliampere-hour) cells, the keyer should operate for many months. The NiCads should be recharged when the voltage drops to about 4.5, or once every six months, whichever comes first.

If ac operation is contemplated, the voltage presented to the keyer should be approximately 5, plus or minus 0.5 volt. The ripple content of the supply should be low. Note that because this keyer draws so little current during standby (10 μA or so), series-connected Zener regulators are difficult to use.

Other Controls

The TUNE/MONITOR/OFF switch (S9) allows the transmitter to be keyed continuously when placed in the TUNE position and selects operation with or without the internal monitor. Operating with the monitor enabled will demand more power from the batteries. Most operators prefer to use the transmitter sidetone instead.

When the AUTO-SPACE feature is enabled, the keyer will perform precision spacing for you. The end result will be more uniform cw.

The WEIGHT control increases the on-to-off time ratio of the generated characters as the control is advanced in a clockwise direction. In the fully counterclockwise position, 50% weighting is provided. The final setting of this control will depend on the keying circuit time constants of the transmitter used and on personal tastes.

Speed Determination

The method used to determine the operational speed of the keyer is based on the fact that the buffers are exactly 512 bauds in length. Here's how it's done. Locate an empty buffer (or one you wish to empty) and press the pushbutton while it is in the LOAD mode. Count the number of seconds it takes until the STATUS LED extinguishes and divide that number into the constant 614.4. That will provide you with the exact speed (in wpm) of the keyer.

Acknowledgments

The authors gratefully acknowledge the efforts of Tom Lindgren (WØWP) and Glenn Thorne (KDØQ) in developing the initial version of the pc board, Joe Gentle (NØBB) for critical evaluation of the keyer "feel," which led to improving it, Russ Lenth (AEØR) for suggesting the addition of D3, and the many hams who have built their own units and expressed satisfaction. We hope you'll join that happy group! QST

Notes

[1]Parts and kits may be obtained from The Partstore, 999 44th St., Marion, IA 52302. Harris HM6504-9 RAMs are also available from your nearest Schweber Electronics distributor. The HM6504-9 has a specified standby current drain of 10 μA (maximum), with 0.1 μA being typical. An HM6504-5 is specified at 500 μA (maximum) and should probably be avoided if battery operation is contemplated.

[2]A comprehensive instruction manual accompanies each bare board or keyer kit. The manual is available separately for $3 postpaid. Please include an s.a.s.e. when requesting information. The ARRL and *QST* in no way warrant this offer.

Strays

TA PROFILES

☐ RFI/TVI headaches? Yes, indeed! Many radio amateurs are confronted with this annoying situation. For this reason, we are pleased to have ARRL Technical Advisor Harold R. Richman, W4CIZ, join our official family. His area of TA expertise is RFI/TVI.

A member of the ARRL since 1931, Hal received his first Amateur Radio license in 1930 and now holds an Extra Class license. He also has Commercial Radiotelephone, First Class and Radiotelegraph Second Class licenses. Active on the high-frequency and 144-MHz bands from his station in Annandale, Virginia, Hal has held appointments as Emergency Coordinator and Official Phone and Relay Stations. He has presented numerous papers on RFI and TVI correction at club meetings, seminars and technical symposiums, and has had many articles published on this subject in *QST* (see May 1981 *QST*) and other journals. He compiled and edited the WTVIC TVI Aids posters and pamphlets for publication.

W4CIZ is a member of the ARRL RFI Task Group, North Virginia Chapter QCWA, OTC, Vienna Wireless Association and is a Life/Senior member of the IEEE, now serving as director of Northern Virginia Section and as advertising manager for the *NOVA Bulletin*.

TA Hal, W4CIZ (right), proud recipient of the ARRL Roanoke Division Service Award, presented by Vic Clark, W4KFC.

Before retiring in 1974, Hal served as Engineer in Charge of the 24th District Office of the FCC, active in inspections, examinations, enforcement, investigative and other responsibilities of a field officer. He was the recipient of three efficiency awards granted by the FCC: a Sustained Superior Accomplishment award, a Superior Accomplishment award and a Special Acts and Services award. Hal holds a Cinematographer rating in the Washington Society of Cinematographers, and he now serves as Director/Historian. He is also active in the American Theatre Organ Society, and has memberships in the National Capital Trolley Museum and the Yogie Magic Club of Baltimore. — *Marian Anderson, WB1FSB*

HOW-TOs FOR K2BSA/4 QSL

☐ For those of you who contacted K2BSA/4 and wish to receive the commemorative QSL card, send your card and an s.a.s.e. to: K2BSA/4, c/o ARRL, 225 Main St., Newington, CT 06111. And, introduce a local Scout to Amateur Radio. — *Steve Place, WB1EYI*

I would like to get in touch with . . .

☐ Travel agents interested in forming a net. Art Lyon, KC4OM, P. O. Box 353, Ocala, FL 32678.